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A Complete Scheme for Creating Predefined Networks of Individual Carbon Nanotubes

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ABSTRACT

We describe and demonstrate a method of creating arrays of patterned, individual, single-walled carbon nanotubes, including the spectroscopic mapping of the array. The process consists of creating networks of nanotubes suspended between silicon pillars, which are then transferred onto other substrates by an innovative process of direct stamping. Raman spectroscopy is used to spatially map and assign the specific properties of the suspended network prior to transfer. This method provides a simple and inexpensive means for deriving nanoscale devices utilizing individually assigned carbon nanotubes in a robust and non-surface-specific technique.

Progress in implementing bottom-up approaches for creating large scale networks of molecular based devices has been hampered by the shear difficulty of screening, manipulating, and patterning elements of nanometer sized dimensions. Consequently, the past few years have heralded many innovative approaches for patterning molecules using various chemical and physical methods, providing proof-of-concept devices based on many new nanomaterials.[1−4]

Carbon nanotubes (CNTs) have spearheaded much of the research in this field and, in particular, in the field of nanocircuits, due to their superb electrical properties, ease of fabrication, and overall stability.[5] Transistors and devices consisting of single-walled carbon nanotubes (SWCNTs) were first demonstrated over a decade ago,[6,7] and a method of patterning large scale networks of SWCNTs, while maintaining their vital properties, has recently been the focus of intense research.[8−11] Despite these efforts, to date, no method has been devised that can address all four crucial aspects involved in the fabrication of large networks of SWCNTs, namely, aligning the SWCNTs in a preset pattern, positioning the nanotubes in a desired location, selecting or identifying the chirality of each of the individual CNTs, and, finally, the ability to integrate such CNT nanocircuits in an integrated circuit (IC) compatible environment. Efforts so far have involved the use of chemical templates to guide solution-based CNTs to desired locations,[11,12] procedures implementing nanostamping of CNT-based devices[13−15] allowing one to directly utilize as-grown nanotubes for devising CNT-based devices, as well as many other techniques.[5,11]

Here we present a complete scheme suited for the production of large CNT arrays with predefined, controlled geometry (i.e., position and alignment) as well as easily determined chirality (i.e., metallic or semiconducting nanotubes). The method can be demarcated into individual stages, which will be addressed sequentially in detail later in the text (schematically presented in Figure 1). The procedure is as follows: First, SWCNTs are grown between microfabricated silicon pillars,[16,17] creating networks of individually isolated, taut,[18] suspended-SWCNTs (susSWCNTs) (Figure 1a). Next, the suspended network is mapped, using Raman spectroscopy (RS), providing vital structural information (i.e., chirality) regarding each of the susSWCNTs (Figure 1b). The entire network of susSWCNTs is then stamped onto a different substrate, transferring the susSWCNTs onto the target substrate, while maintaining the array structure imparted by the initial suspended network (Figure 1c). The susSWCNTs can be stamped either directly onto a target containing an underlying electronic infrastructure or onto

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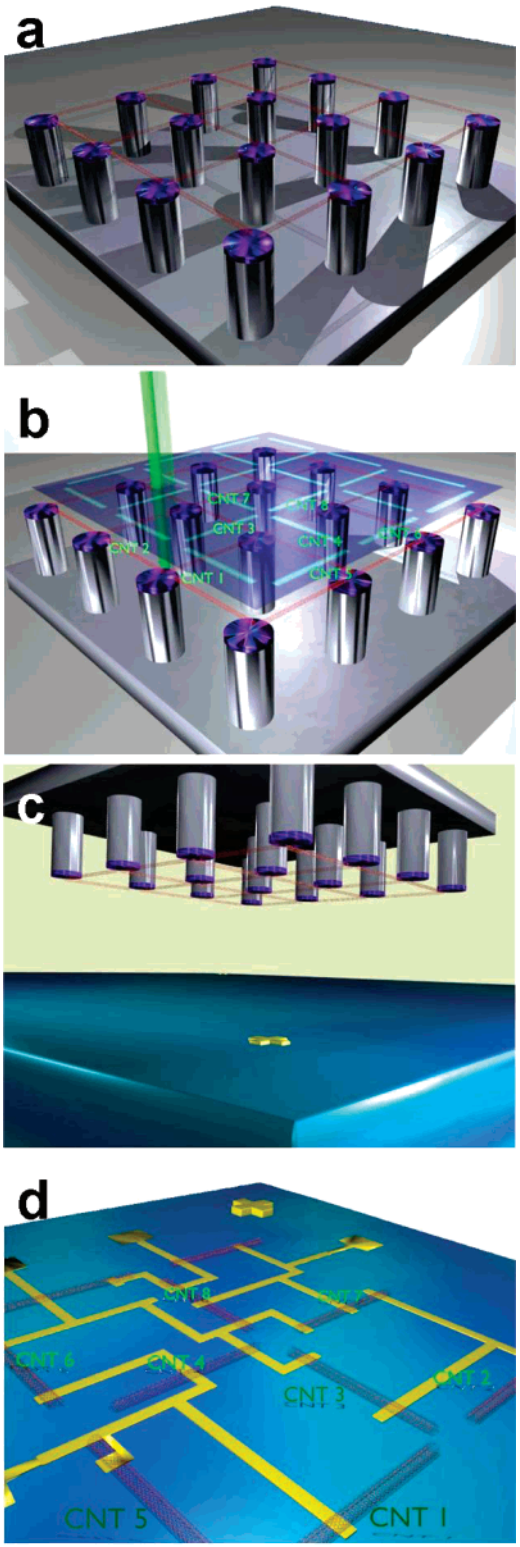

Figure 1. (a) Carbon nanotubes grown between microfabricated silicon pillars, creating a tightly bound, orderly suspended network. (b) Raman mapping of the suspended network, providing information regarding each individual suspended nanotube. Mapping is schematically represented as corresponding with the suspended network. Information regarding each individual nanotube can be isolated and stored, as indicated by the labels. (c) Imprinting the suspended network onto a target surface, with alignment marks. (d) Electronic circuit containing carbon nanotubes stamped directly onto a matching arrangement of electrodes. Information regarding each isolated nanotube (as labeled) correlates with the Raman mapping.

clean surfaces, with the circuitry added later, using standard micro- and nanofabrication procedures (Figure 1d). This innovative stamping method allows one to simultaneously arrange numerous SWCNTs in a distinct pattern, with the combined Raman spectroscopy assigning specific properties to each individual nanotube, and the capability of destroying individual nanotubes with the same Raman laser system.[19] With this method, large networks of CNTs (consisting of hundreds of CNTs) have been realized, containing long segments of straight SWCNTs (∼5−20 μm long each), which are devoid of defects. Furthermore, the method is not limited by the target substrate chosen and is perfectly compatible with either polymeric or IC-derived substrates.

Turning to the individual steps entailed, the first step involves the creation of arrays of silicon dioxide capped silicon pillars from a silicon wafer (500 nm of SiO_2 on 450 μm thick silicon), which can be prearranged to fit the pattern of the desired device architecture. This process has already been reported by others,[16,17] demonstrating the ability to create orderly formations of suspended CNT arrays. However, the latent capabilities of this arrangement have as of yet not been fully realized. Here, 20 μm high pillars of silicon, with various spacing, diameters, and geometries, were fabricated using standard microfabrication techniques. After fabrication, the pillar tops were coated with a catalyst and then heated in a chemical vapor deposition (CVD) furnace, producing networks of susSWCNTs. Figure 2a is a high-resolution scanning electron microscope (HRSEM) image illustrating susSWCNT networks (additional images appear in the online Supporting Information). The most conspicuous detail of the suspended network is the ordering and tension of the susSWCNTs, which has been described and explained elsewhere,[18,20,21] and is caused by the strong forces binding the nanotubes to the pillar tops, as well as to each other, pulling the slack segments against the edges of the pillar top, until they are taut.

As there is currently no technique to selectively grow SWCNTs with specific properties directly on a substrate, obtaining structural information of individual SWCNTs using RS[22] has been shown to be particularly important and useful. RS can provide the chiral indices of a SWCNT, relating its most crucial structural properties. The detection of SWCNTs in their suspended state supplies a considerably stronger signal than those lying upon a surface,[23−25] due to the stronger internal molecular vibrations of the free tube[23] as well as a stronger contrast compared to the background noise of a molecule on a surface. In an individual RS spectrum, the location of each resonant mode is highly dependent upon the diameter of the SWCNT measured, and a direct, empirical correlation can be found between the SWCNT diameter and the location of each peak.[22] A typical Raman spectrum contains a few notable peaks, in particular, are the G-band of a CNT, which is a measure of the vibrations in the graphene sheets of the CNT wall, and which appears at a near constant value of ∼1590 cm^{-1}, and the radial breathing mode (RBM), which is highly dependent upon the CNT diameter.

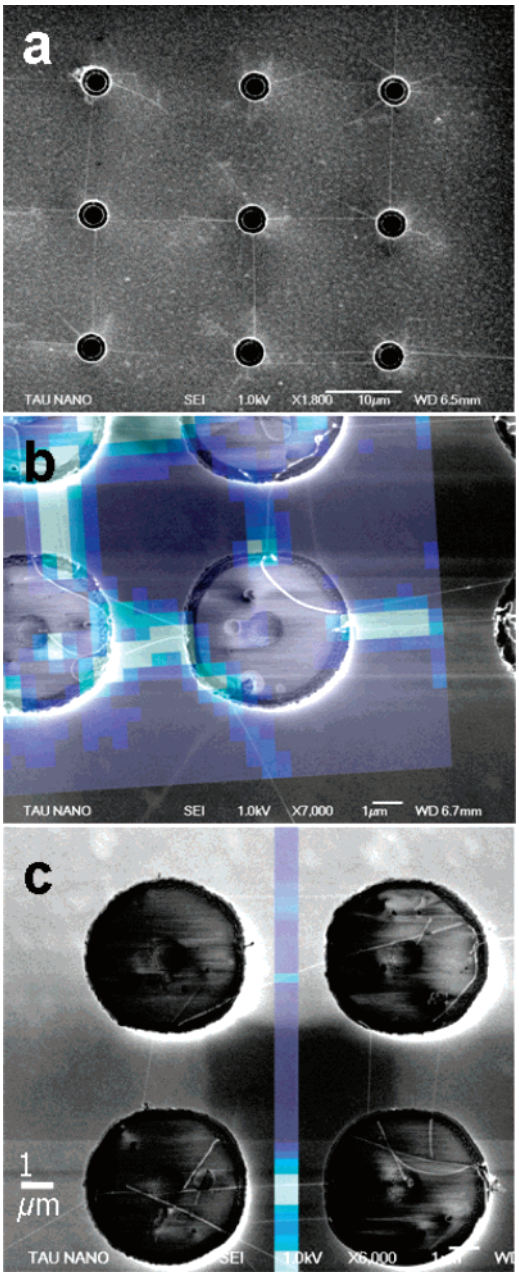

Figure 2. (a) Scanning electron microscope images of suspended carbon nanotubes bridging the gaps between 20 μm high silicon pillars. Pillars here are 4 μm in diameter. The suspended nanotubes are strikingly taut and usually bridge the space between two neighboring pillars. (b) Overhead HRSEM image of four silicon pillars, with bridging nanotubes, along with a Raman mapping of a portion of the same image, superimposed. The brighter pixels in the Raman mapping correspond to a higher intensity of the G-band spectral line. The brighter pixels can be seen to follow the contours of the suspended nanotubes. (c) A line mapping, showing a one-dimensional line displaying the same pixelized Raman spectroscopy information. The nanotube at the top (as seen in the underlying image) is out of focus.

Before being stamped onto another surface, information regarding the properties of each susSWCNT is vital if the intrinsic properties of each SWCNT are to be utilized to their fullest. In fact, mapping suspended networks of CNTs can be used both to determine the structure of each susSWCNT and to provide the spatial identification of each isolated susSWCNT, as has been previously been demonstrated by others.[26,27] By isolating one of the spectral peaks (in this case, the G-band, since it has the largest intensity), one can spatially raster the areas between the pillars, obtaining a strong peak signal (per pixel) corresponding to each suspended CNT.[27] The relative intensity of the G-band spectral line can also supply information distinguishing metallic and semiconducting nanotubes.[22] Parts b and c of Figure 2 display two such mappings, taken with an in-house-built Raman microscope. Figure 2b displays an overlay of an HRSEM image (showing pillars similar to those in Figure 2a), with part of the RS mapping superimposed. The brighter pixels of the mapping correspond to stronger values of the measured G-band intensity and can clearly be seen to correspond to the locations of the susSWCNTs. In addition, as can be seen from the upper left portion of the pillar in the center of Figure 2b, the RS G-band peak intensity is greatly reduced when the nanotube is attached to the pillar top, whereas it is easily visible once the CNT disengages from the pillar. This is in contrast to the HRSEM image, whereupon the CNTs are in better contrast when in contact with the pillar top. Figure 2c demonstrates a different type of RS mapping. Here, a line-mapping scheme is used, displaying peaks only in the vicinity of the susSWCNTs. In this image, the susSWCNT at the top of the image (seen in the underlying HRSEM image) is barely visible in the RS mapping since it is out of the RS laser focus, indicating that the susSWCNT is not suspended in the same plane as the pillar tops and may therefore not be in contact with the target substrate upon transfer.

Mapping the susSWCNTs using a Raman-based system is therefore ideal for this proposed scheme as it provides a number of advantageous capabilities. With the suspended network mapped prior to stamping, the time-consuming analysis of the susSWCNTs using the HRSEM can be avoided, with the Raman mapping imparting precise locations of bridging susSWCNTs, as well as simultaneously conveying the relevant structural information of each individual nanotube. A fully integrated system would use the RBM mode rather then the G-band, which was used here for demonstration purposes only.

The transferring of nanotubes from the pillars onto various substrates is similar to previously demonstrated stamping methods;[13,14] however the process is augmented here by the capability of transferring complete *networks* of discrete SWCNTs. This permits the one-step transference of hundreds of spatially isolated and defined tubes (as opposed to single CNT transfer methods previously reported[26]). The transfer here was achieved by the addition of a small amount of deionized water (DI water) and heating the target substrate (SiO_2) on a conventional hot plate to ~150−200 °C, at which point the source substrate (pillars) is firmly pressed against the target substrate for a short duration. The addition of DI water was empirically found to facilitate the transfer of the susSWCNTs onto the target surface, while "dry" stamping resulted in hardly any transferred nanotubes. The effect of the solvent may tentatively be associated with capillary-like forces that help bind the suspended SWCNT segments to the target surface. Stamping onto silicon, silicon nitride, and

gold substrates was also demonstrated, with comparable results, with only the results on silicon dioxide presented here.

Images of transferred networks of CNTs are displayed in parts a and b of Figure 3. Here, the spatial relation to the original stamp, as well as the straightness of the stamped tubes, a property which is imparted by the nature of the susSWCNTs, is seen. Positions of the pillars (and comblike structures) are identified by the residue they leave on the surface (dotted lines in Figure 3a). The geometry of the comblike structure seen in the inset of Figure 3a results in CNTs bridging between the fingerlike structures, thereby determining the distance between the segments of SWCNTs in the stamped substrate (in this case, 25 μm, as signified by the white arrow). The transfer procedure occasionally leaves an imprint of the nanotubes from the pillar tops, as can be seen by the white disks in Figure 3b. Each disk is actually a mesh of transferred SWCNTs, which were confined to the pillar tops, with the straight segments of parallel susSWCNTs seen extending between the transferred islands.

To further demonstrate that the nanotubes transferred are of the single-walled variety, a sample of susSWCNTs was transferred directly onto a transmission electron microscope (TEM) grid comprised of a thin silicon nitride membrane with holes.[18] Figure 3c shows TEM images (200 kV beam) of a SWCNT transferred onto a holey nitride grid. The individual SWCNT bridging over one of the holes in the grid is distinctly visible. Imprinting the susSWCNTs directly onto these fragile membrane grids displays yet another capability of the method employed, demonstrating the versatility of the target substrates applicable.

Creating large-scale circuits using the stamped SWCNTs can be implemented either by stamping the nanotubes directly onto preexisting device architectures or by stamping them onto clean substrates and adding the circuitry afterward. Both of these techniques were used in this study. In Figure 4a, a very long and straight nanotube, imprinted onto a clean silicon dioxide substrate (500 nm thick on p-type silicon) was contacted after imprinting by using e-beam lithography. Cr−Au electrodes (8 and 20 nm, respectively) and the underlying silicon were used to measure typical SWCNT transistor characteristics with a drain−source voltage of 100 mV. Figure 4b displays a semilogarithmic $I-V$ curve of a p-type, SWCNT transistor, with a 0.5 μm channel length (the leftmost set of electrodes in Figure 4a), with the electrodes added after imprinting. The on−off gain ratio of this transistor was of 2 orders of magnitude, with a saturation current of 0.8 μA, and a residual off current of 3 nA. Figure 4c displays a semilogarithmic $I-V$ curve for a p-type, SWCNT transistor fabricated by placing an individual SWCNT between two *existing* electrodes (image not shown), with a 4 μm channel length. Here, the on−off gain ratio was over 4 orders of magnitude, with a saturation current of 0.1 μA and an off current of a few picoamperes. The discrepancy in the performances of these transistors may be due to the difference in work functions of the metal in contact with the nanotube (4.5 and 5.1 eV for chrome and gold, respectively): In the first case, with the electrodes placed after the SWCNTs were transferred (Figure 4b), chrome was in contact with the SWCNT, whereas in the latter case

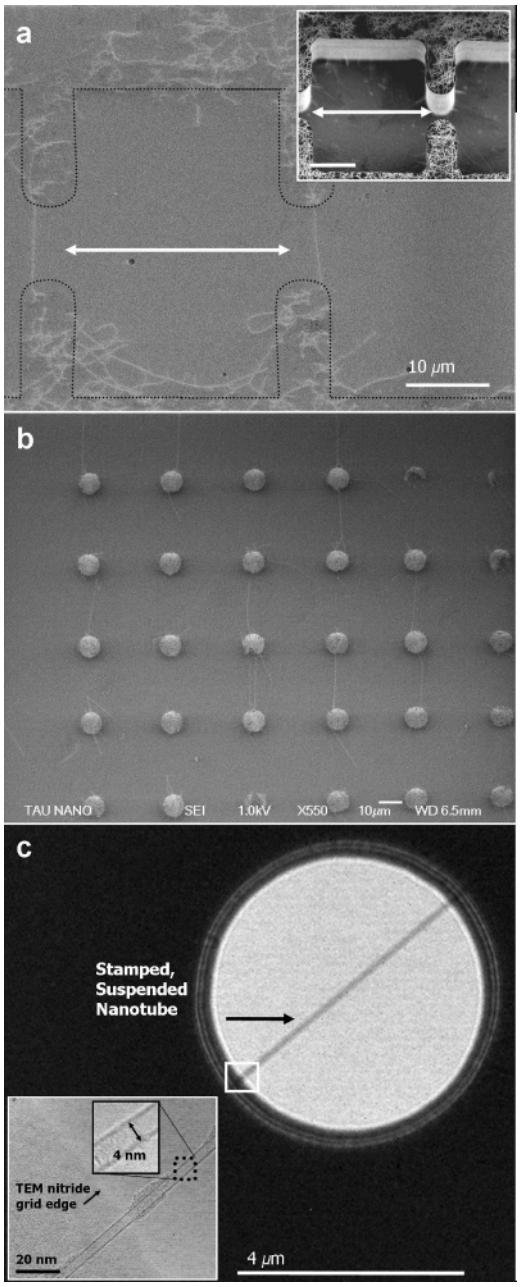

Figure 3. (a) HRSEM images of nanotubes transferred from a comblike structure onto SiO_2. The distance between nanotubes is 25 μm, as defined by the spacing in the original template (demonstrated by the white arrow between the straight nanotube segments). The dotted black line is a visual aid representing the contours of the original stamp. Inset: Isometric HRSEM image of the original comblike template, with bridging nanotubes. Scale bar: 10 μm. (b) A large set of parallel-stamped nanotubes. White disks (high-density transferred CNTs) represent the locations of the original pillar tops. (c) An out-of-focus TEM image of a nanotube stamped directly onto a holey nitride grid, with one of the nanotubes suspended over one of the holes in the TEM grid. Inset: A high-resolution close-up of the edge of the hole, with the suspended nanotube, displaying the high contrast walls of the single-walled nanotube. Included is also a close-up of the nanotube, showing its true diameter.

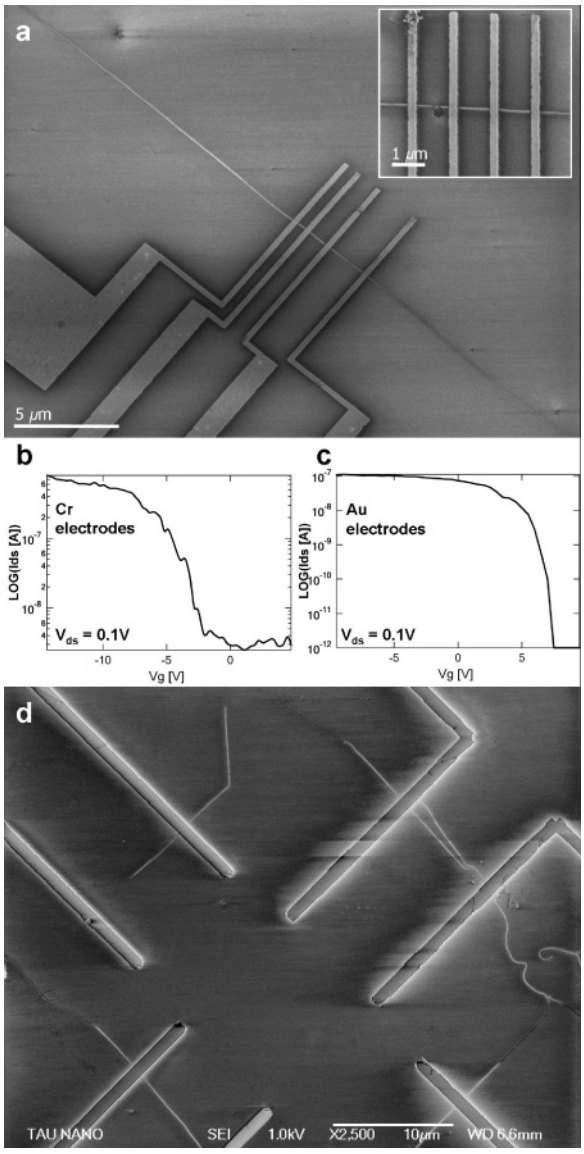

Figure 4. (a) HRSEM image of electrodes placed on a long, straight, stamped segment of nanotube. Electrodes here were placed at varying distances over the nanotube (0.5, 1, and 1.5 μm). Inset: Another close-up image of equally spaced electrodes over a stamped nanotube (1 μm spacing). (b) Electrical characteristics a nanotube transistor (0.5 μm channel), with the electrodes (CrAu) deposited after the nanotubes had been stamped onto a silicon oxide surface. (c) Electrical characteristic of a transistor fabricated by placing an individual nanotube directly onto two existing (CrAu) contacts (4 μm channel). (d) HRSEM image of a patterned CNT device architecture system created using the stamping method described in the text. The squarelike formation of the nanotubes originates from the square array of pillars.

(Figure 4c), the SWCNTs were placed directly onto gold. The different surface properties of the two samples may also contribute to the observable shift in the threshold voltage. Overall, these CNT transistors demonstrate characteristics comparable with contemporary SWCNT transistors derived using other methods.

Figure 4d demonstrates a complex device architecture that is easily obtainable using the methods described above. This image displays the advantageous use of stamping multiple nanotubes in a prearranged pattern, with perpendicular SWCNTs transferred in a single step. Characterizing such devices is currently underway.

The results presented here demonstrate several novel aspects of carbon nanotube field effect transistors fabrication, as well as supplying a systematic approach for fabricating large quantities of CNT-based devices on various substrate materials. By integrating both the stamping method presented, as well as the RS mapping, one can quickly and inexpensively create large arrays of CNT devices, while simultaneously acquiring the chiral indices of each of the stamped nanotubes. The advantages of this scheme are plentiful, including the use of defect-free, long SWCNTs grown in the suspended state, the precise structural information related by the Raman mapping, the simple, one-shot procedure enabling the creation of an entire prearranged network of individual SWCNTs, and the length of the straight, stamped, nanotube segments. Further modifications of the scheme could include chirality-controlled CVD growth of CNTs by selectively choosing the catalysts[28] deposited on the pillar tops, as well as better control of both the yield and directionality of the SWCNTs between the pillars,[18] and removal of stray nanotubes.[19] In terms of transistor properties, one can tailor the sensitivity of each parallel array of transistors (on each nanotube segment) to the specifications of each nanotube. It has been shown that different chiralities of SWCNTs react differently to different types of chemicals and can be wrapped by different segments of DNA.[29,30] By knowing the chiralities and locations of each SWCNT in a circuit, one can envision the construction of CNT-based sensors and DNA chips. Therefore, the a priori identification of the individual SWCNTs on the target surface can also be utilized for creating complex CNT-based sensor arrays, without further modification of the circuit.

This scheme provides a comprehensive and scalable technique for creating large scale devices, pending optimization of the individual processes described. The major limitations lie in the yield of transferred tubes and in the initial growth of the network of CNTs between the initial pillars. Using our liquid-based catalyst deposition, we have achieved nearly 100% yields of CNTs between neighboring pillars; however, this also leads to the growth of more than one CNT between each pillar.[31] The solution to this problem is a matter of pillar geometry: small pillar tops will yield fewer stray CNTs, and larger spacing (>20 μm) accomplishes a further filtration. Further investigation of improving the initial network growth is currently under investigation; nevertheless, the integration of the technique described here is already being implemented by us for use with various device architectures.

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Supporting Information Available: Descriptions of pillar fabrication, CVD growth, imaging and spectroscopic equipment, the stamping method, electrical measurements, suspended CNT growth, and stamping results. This material is available free of charge via the Internet at http://pubs.acs.org.

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(31) Yields of bridging nanotubes approaching 100% were particularly attainable between pillars with the CNTs bridging the gap between them in the direction of the gas flow within the CVD tube furnace. However, SWCNTs growing in a perpendicular direction to the gas flow were also found in large numbers. Creating smaller pillar tops, as in ref 17, enables one to limit the number of suspended SWCNTs, and many arrays of suspended SWCNTs, with nearly unitary SWCNTs between the pillars, were created upon smaller fabricated pillars. Furthermore, by incorporating the methods implied in ref 20, one should be able to further optimize the method described here.

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